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EXAMINER	
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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/410,642	Applicant(s) EDWARDS ET AL.
	Examiner Michael C Maskulinski	Art Unit 2113

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 21-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 21-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final Office Action

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-6, 11-13, 15-18, 21, 22, and 25-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Wolff et al., U.S. Patent 4,486,826.

Referring to claims 1, 22, 33, and 34:

a. In column 3, lines 61-64, Wolff et al. disclose that the A and B buses each carry an address (packet routing information).

b. In column 3, lines 61-64, Wolff et al. disclose that the A and B buses each carry an identical set of cycle definition, address, data, parity and other signals that can be compared to warn of erroneous information transfer between units (packets of information, wherein each packet comprises a number of fields containing information).

c. In column 14, lines 7-8, Wolff et al. disclose that each data transfer cycle has at least four such timing phases. Further, in column 14, lines 28-68 continued in column 15, lines 1-45, Wolff et al. disclose a definition phase

containing address information and a response phase containing data. By definition a packet is a group of bits that perform a function. In Wolff et al. a cycle is a group of bits with different phases that perform a single function. Therefore, Wolff et al. teach a packet containing information including both data and packet routing information. Further, in column 14, lines 45-58, Wolff et al. teach that each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data.

d. In column 2, lines 31-35, Wolff et al. disclose a computer system (a functional circuit), which has a processor module with a processing unit, a random access memory unit, and peripheral control units (plurality of modules), and it has a single bus structure which provides all information transfers between the several units of the module (interconnect for information transfer).

e. In column 2, lines 31-35, Wolff et al. disclose that the computer system has a single bus structure, which provides all information transfers between the several units of the module (circuitry for receiving at least part of said information).

f. In column 2, lines 48-56, Wolff et al. disclose that the computer system provides fault detection at the level of each functional unit within a processor module. To attain this feature, error detectors monitor hardware operations within each unit and check information transfers between the units (circuitry for

determining if said at least part of said information satisfies one or more conditions).

g. In column 2, lines 48-56, Wolff et al. disclose that the detection of an error causes the processor module to isolate the bus or unit which caused the error from transferring information to other units (circuitry for performing one or more actions in response to the determination that at least part of the information satisfies one or more conditions).

Referring to claim 2, in column 11, lines 36-54, Wolff et al. disclose that in response to the fault signal, the control section produces an error signal (trace message) that the X bus transmits to all units of the module.

Referring to claims 3 and 4, in column 11, lines 50-54, Wolff et al. disclose that any failing unit also produces an interrupt signal that causes the central processing unit of the module (one or more CPUs) to interrogate the different units to locate the faulty one.

Referring to claim 5, in column 2, lines 48-56, Wolff et al. disclose that the detection of an error causes the processor module to isolate the bus or unit which caused the error from transferring information to other units (prevent one or more modules from being granted access to the interconnect).

Referring to claims 6 and 11, in column 40, lines 63-68 continued in column 41, lines 1-2, Wolff et al. disclose a broken flip-flop to disable the drivers of a peripheral device in response to a fault.

Referring to claim 12, in column 40, lines 56-68 continued in column 41, lines 1-2, Wolff et al. disclose a comparator that compares peripheral (module) output signals (information on interconnect) with corresponding output signals from the check control section (match conditions). In response to an invalid comparison, the comparator switches a so-called broken flip-flop to disable the drivers (determining circuitry using a comparator).

Referring to claims 13 and 15, in column 25, lines 32-40, Wolff et al. disclose that the central processing unit (circuit) has two subsystems and control circuits within the unit that take the unit off-line upon detection of an error (precondition: enabled or not enabled). Further, in column 40, lines 56-68 continued in column 41, lines 1-2, Wolff et al. disclose a comparator that compares peripheral (module) output signals (information on interconnect) with corresponding output signals from the check control section (match conditions). In response to an invalid comparison, the comparator switches a so-called broken flip-flop to disable the drivers (determining circuitry using a comparator).

Referring to claims 16 and 17, in figures 5A, 5B, and 1, and in column 28, lines 21-35, Wolff et al. disclose latch 120 which is between the interconnect and the processor module (circuitry external to said circuit). The latch provides temporary storage of output data so that in the event any error is reported on the buses, the operating sequence in which the error was reported can be duplicated and the data retransmitted on the A bus 42 (external circuitry is enabled).

Referring to claims 18 and 21, in column 3, lines 57-68, Wolff et al. disclose that the bus carries cycle-definition (type of transaction to which the information relates), address (address of the information), data, parity, and other signals that can be compared to warn of erroneous information transfer between units (match conditions). The information comprising packets of information, requests, and response is inherent to the information mentioned above that is sent over a bus.

Referring to claim 25, in column 20, lines 35-55, Wolff et al. disclose an arbitration network (arbiter) which provides an automatic hardware determination of which unit, or pair of partner units, that requests access to the bus structure (interconnect) has priority to initiate an operating cycle (granted access).

Referring to claim 26, in column 20, lines 35-55, Wolff et al. disclose that the processor module (determining circuitry) has two arbitration networks (arbiter) connected to bus A and bus B.

Referring to claims 27 and 31, in column 3, lines 34-47, Wolff et al. disclose that upon detection of an error-manifesting fault in any unit, that unit is isolated and placed off-line so that it cannot transfer information to other units of the module. The partner of the off-line unit continues operating and thereby enables the entire module to continue operating, normally with essentially no interruption.

Referring to claim 28, in the abstract, Wolff et al. disclose a bus.

Referring to claims 29, 30, and 32, in column 2, lines 48-63, Wolff et al. disclose error detectors (debug module) at the level of each functional unit (module). Further, in column 40, lines 63-68 continued in column 41, lines 1-2, Wolff et al. disclose a

comparator, which switches a so-called broken flip-flop to disable the drivers upon detection of an error (circuitry for performing at least one action). The comparator is part of the control unit, which is part of the functional unit (circuitry in said debug module).

3. Claims 1, 22, 33, 34, 35 and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Goodrum et al., U.S. Patent 6,032,271.

Referring to claims 1, 22, 33, 34, 35, and 36:

a. In the Abstract, Goodrum et al. disclose a bus with devices connected to it (an interconnect and a plurality of modules connected to said interconnect for putting packets of information onto the interconnect).

b. In Figure 15A and the table in column 14, Goodrum et al. disclose that each packet comprises a number of fields containing information including both data and packet routing information, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data).

c. In column 45, lines 16-40, Goodrum et al. disclose that when a transaction on the PCI bus does target the QPIF, the slave state machine enters a SLAVE_DAC dual address cycle state if the p2q_ dac_flag is asserted and an address parity error has not occurred (p2q_perr_is low). If the transaction is not a dual address cycle and is a posted memory write request, and if a parity error has not occurred in the address phase, the slave state machine loads the write counters (i.e., asserts load_write_counter) and determines whether it can accept

the transaction (circuitry for receiving at least part of said information; circuitry for determining if said at least part of said information satisfies one or more conditions; and circuitry for performing one or more actions in response to the determination that at least part of the information satisfies one or more conditions).

d. Fields containing information, including a routing field, and address field, a source field, a transaction type field, a transaction identifier field, and an operation code field are inherent to the PCI bus of Goodrum et al.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S Patent 4,486,826 as applied to claim 6 above, and further in view of Cepulis, U.S. Patent 6,055,596.

Referring to claim 7, in column 40, lines 63-68 continued in column 41, lines 1-2, Wolff et al. disclose a so-called broken flip-flop to disable the drivers of a peripheral device (module) in order to prevent it from putting further information onto the bus (interconnect). However, Wolff et al. don't explicitly disclose using a register for preventing a module from putting information onto the interconnect. In column 75, lines 3-10, Cepulis discloses that the CPU can power up one of the slots by writing a "1" to a corresponding bit of a slot enable register and disable the slot by writing a "0" to this bit.

It would have been obvious to one of ordinary skill at the time of the invention to include the slot enable register of Cepulis into the system of Wolff et al. A person of ordinary skill in the art would have been motivated to make the modification because as disclosed by Wolff et al. a switching means is needed to disconnect a peripheral device. The slot enable register of Cepulis is one type of switching means used to disconnect a peripheral device.

Referring to claim 8, in column 75, lines 3-10, Cepulis discloses that the CPU can power up one of the slots by writing a "1" to a corresponding bit of a slot enable register and disable the slot by writing a "0" to this bit (the register comprises one bit for each module and the value of said bit determines if the respective module is prevented from putting further information into the interconnect).

Referring to claim 9, in column 75, lines 3-10, Cepulis discloses that the CPU (one module arranged to access the register non-intrusively) can power up one of the slots by writing a "1" to a corresponding bit of a slot enable register and disable the slot by writing a "0" to this bit.

Referring to claim 10, in column 75, lines 3-10, Cepulis discloses a slot enable register with a corresponding bit for each slot (the location being independent of the address of the module).

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S. Patent 4,486,826 as applied to claim 13 above, and further in view of Ardini, Jr. et al., U.S. Patent 4,918,693. In column 40, lines 56-68 continued in column 41, lines 1-2, Wolff et al. disclose a comparator that compares peripheral (module) output signals

(information on interconnect) with corresponding output signals from the check control section (match conditions). In response to an invalid comparison, the comparator switches a so-called broken flip-flop to disable the drivers (determining circuitry using a comparator). However, Wolff et al. don't explicitly disclose satisfying a precondition by having match conditions occurring a predetermined number of times. In column 8, lines 9-14, Ardini, Jr. et al. disclose a diagnostic program that, after a certain number of parity error signals are received from board 202, it will send a code to disable the parity check circuit output. It would have been obvious to one of ordinary skill at the time of the invention to include the parity error signal threshold of Ardini, Jr. et al. into the system of Wolff et al. A person of ordinary skill in the art would have been motivated to make the modification because a parity check circuit can become faulty so that it continuously generates a parity error signal on its output (see Ardini, Jr. et al.: column 8, lines 7-9). In this case, to check for a faulty parity circuit would require a precondition.

7. Claims 19 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S. Patent 4,486,826 as applied to claim 1 above, and further in view of Pizzica, U.S. Patent 5,652,754.

Referring to claims 19 and 35, in column 2, lines 48-56, Wolff et al. disclose that the computer system provides fault detection at the level of each functional unit within a processor module. To attain this feature, error detectors monitor hardware operations within each unit and check information transfers between the units (circuitry for determining if said at least part of said information satisfies one or more conditions). Further, in column 3, lines 61-64, Wolff et al. disclose that the A and B buses each carry

an identical set of cycle definition, address, data, parity and other signals that can be compared to warn of erroneous information transfer between units (packets of information). However, Wolff et al. don't explicitly disclose storing circuitry to store the information which satisfies the at least one condition. In column 2, lines 53-60, Pizzica discloses a signature storage device that stores a fault free signature from a functional digital module and faulty signatures obtained by shorting and opening each of the circuit nodes thereof. It would have been obvious to one of ordinary skill at the time of the invention to include the faulty signature storing of Pizzica into the system of Wolff et al. A person of ordinary skill in the art would have been motivated to make the modification because *the recorded signatures can be used for subsequent pass/fail determination of digital modules that are tested* (see Pizzica: column 1, lines 46-48).

Further, referring to claim 35:

a. In column 3, lines 61-64, Wolff et al. disclose that the A and B buses each carry an address (packet routing information).

b. In column 14, lines 7-8, Wolff et al. disclose that each data transfer cycle has at least four such timing phases. Further, in column 14, lines 28-68 continued in column 15, lines 1-45, Wolff et al. disclose a definition phase containing address information and a response phase containing data. By definition a packet is a group of bits that perform a function. In Wolff et al. a cycle is a group of bits with different phases that perform a single function. Therefore, Wolff et al. teach a packet containing information including both data and packet routing information. Further, in column 14, lines 45-58, Wolff et al.

teach that each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data.

c. In column 2, lines 31-35, Wolff et al. disclose a computer system, which has a processor module with a processing unit, a random access memory unit, and peripheral control units (plurality of modules), and it has a single bus structure which provides all information transfers between the several units of the module (interconnect for information transfer).

d. In column 2, lines 31-35, Wolff et al. disclose that the computer system has a single bus structure, which provides all information transfers between the several units of the module (circuitry for receiving at least part of said information).

e. In column 2, lines 48-56, Wolff et al. disclose that the computer system provides fault detection at the level of each functional unit within a processor module. To attain this feature, error detectors monitor hardware operations within each unit and check information transfers between the units (circuitry for determining if said at least part of said information satisfies one or more conditions).

8. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S. Patent 4,486,826 as applied to claim 22 above, and further in view of Bershteyn et al., U.S. Patent 5,678,028.

Referring to claim 23, in the abstract, Wolff et al. disclose a fault-tolerant computer system comprising a processor unit, a memory unit, one or more peripheral control units, and a bus structure. However, Wolff et al. don't explicitly disclose that these circuits are an integrated circuit. In the Background of Bershteyn et al., a system-on-a-chip debugger is disclosed. It would have been obvious to one of ordinary skill at the time of the invention to make the system of Wolff et al. into the system-on-a-chip debugger of Bershteyn et al. into the. A person of ordinary skill in the art would have been motivated to make the modification because an entire system can be fabricated on a single wafer decreasing the cost of the entire system (see Bershteyn et al.: column 1, lines 45-67).

Referring to claim 24, in the abstract Wolff et al. disclose a computing module (external module), one or more peripheral control units (modules), and a bus structure (interconnect).

9. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S. Patent 4,486,826, and further in view of Merrill et al., U.S. Patent 4,942,552.

Referring to claim 36:

a. In column 3, lines 61-64, Wolff et al. disclose that the A and B buses each carry an identical set of cycle-definition, address, data, and parity signals. However, Wolff et al. don't explicitly disclose having fields/signals that contain information including a source field, a transaction type field, a transaction identifier field, and an operation code field. In column 7, lines 26-30, Merrill et al. disclose that both the read commands and the write commands contain

parameters which specify the data to be moved, including the source address, destination address, and the length of data to be moved. In column 19, lines 42-50, Merrill et al. disclose an ID field that contains an operation code which identifies one command message from said predetermined set of command messages. In column 23, lines 22-25, Merrill et al. disclose remote command messages including at least first and second remote command message types. In column 11, lines 18-21, Merrill et al. disclose a transaction number that is included in both the output message and the reply to match up the commands and responses. It would have been obvious to one of ordinary skill at the time of the invention to include the fields of Merrill et al. into the system of Wolff et al. A person of ordinary skill in the art would have been motivated to make the modification because these fields can be used to in comparison to other signals so as to warn of erroneous information transfer between units (see Wolff et al.: column 3, lines 63-64).

b. In column 2, lines 31-35, Wolff et al. disclose a computer system (a functional circuit), which has a processor module with a processing unit, a random access memory unit, and peripheral control units (plurality of modules), and it has a single bus structure which provides all information transfers between the several units of the module (interconnect for information transfer that is not a circuit-switched bus).

c. In column 14, lines 7-8, Wolff et al. disclose that each data transfer cycle has at least four such timing phases. Further, in column 14, lines 28-68

continued in column 15, lines 1-45, Wolff et al. disclose a definition phase containing address information and a response phase containing data. By definition a packet is a group of bits that perform a function. In Wolff et al. a cycle is a group of bits with different phases that perform a single function. Therefore, Wolff et al. teach a packet containing information including both data and packet routing information. Further, in column 14, lines 45-58, Wolff et al. teach that each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data.

d. In column 2, lines 31-35, Wolff et al. disclose that the computer system has a single bus structure, which provides all information transfers between the several units of the module (circuitry for receiving at least part of said information).

e. In column 2, lines 48-56, Wolff et al. disclose that the computer system provides fault detection at the level of each functional unit within a processor module. To attain this feature, error detectors monitor hardware operations within each unit and check information transfers between the units (circuitry for determining if said at least part of said information satisfies one or more conditions).

f. In column 2, lines 48-56, Wolff et al. disclose that the detection of an error causes the processor module to isolate the bus or unit which caused the error from transferring information to other units (circuitry for performing one or more

actions in response to the determination that at least part of the information satisfies one or more conditions).

Response to Arguments

10. Applicant's arguments filed July 15, 2003 have been fully considered but they are not persuasive.

11. On page 8, under the section A. The Rejection of Claims under 102 (b), the Applicant argues, "Independent claims 1, 22, 33, and 34 have been amended to clarify that the information packets comprise both data and packet routing information that identifies at least one module associated with the data on the interconnect. In contrast, *Wolff* only (emphasis by Applicant) describes a multi-phase process that has a definition and response phase to establish a connection between a bus master and slave unit, always followed by a data transfer phase for transferring data between the units. See *Wolff*, col. 14, line 44 to col. 15, line 17. There is no routing information associated with the data transferred between the master bus and slave unit in Wolff because a connection between the units was established by in the previous cycle (i.e., the definition and response phase)." The Examiner respectfully disagrees. The Applicant is once again reminded that the definition of a packet in its broadest sense is a serial stream of clocked data bits. In this case a transfer cycle as defined by Wolff et al. would be a packet. Further, the Examiner would like to note that a cycle is four phases and is done over many clock cycles (see Wolff et al.: column 13, line 63 through column 14, line 20). It is well known that a packet, when it is processed, is broken into chunks of

bits that are processed on different clock cycles. Each phase in the cycle can be considered a chunk of bits. Since there is a phase containing the routing information and a phase containing data, all of which contained in a single cycle, then Wolff et al. teach a packet containing information including both data and packet routing information.

12. On page 9, under the section A. The Rejection of Claims under 102 (b), the Applicant argues, "there is nothing that inherently describes or even suggests the address information in *Wolff* includes packet routing information that identifies at least one module on the interconnect." The Examiner respectfully disagrees. In column 14, lines 49-51, Wolff et al. disclose that the bus master unit asserts the physical address signals identifying the memory or **I/O location** for the cycle.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1:136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (703) 308-6674. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MM

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